Enrollment No./Seat No.:

GUJARAT TECHNOLOGICAL UNIVERSITY

MASTER OF ENGINEERING - SEMESTER - II EXAMINATION - WINTER 2025

Subject Code: ME02000181 **Date: 02-01-2026**

Subject Name: VLSI Testing

Time: 02:30 PM TO 05:00 PM **Total Marks: 70**

Instructions

1. Attempt all questions.

2. Make suitable assumptions wherever necessary.

3. Figures to the right indicate full marks.

			Marks
Q.1	**(a)**	Explain the importance of VLSI testing at different abstraction levels.	**07**
	(b)	Discuss various challenges faced during VLSI testing and their solutions.	**07**
Q.2	**(a)**	Describe the concept of Design for Testability (DFT) and its need in modern VLSI systems.	**07**
	(b)	Explain the architecture and design flow of scan-based testing. Provide a neat diagram.	**07**
		OR	
	(b)	Compare different scan cell architectures and explain their design rules.	**07**
Q.3	**(a)**	Define controllability and observability. How are these parameters calculated for a given circuit?	**07**
	(b)	Explain logic and fault simulation with examples. Discuss the role of fault models.	**07**
		OR	
	(a)	Describe various fault simulation techniques and compare their advantages.	**07**
	(b)	Explain the role of RTL design for testability.	**07**
Q.4	**(a)**	Explain the process of Automatic Test Pattern Generation (ATPG) for combinational circuits using Boolean difference.	**07**
	(b)	Describe the working of a sequential ATPG and its limitations.	**07**
		OR	
	(a)	Discuss various algorithms for test pattern generation and untestable fault identification.	**07**
	(b)	Differentiate between deterministic, random, and hybrid ATPG approaches.	**07**
Q.5	**(a)**	Explain the concept of Logic Built-In Self-Test (BIST). Discuss its design rules and architectures.	**07**
	(b)	Describe the importance of fault coverage enhancement and timing control in BIST design.	**07**
		OR	

(a)	Explain Test Pattern Generation and Output Response Analysis techniques in BIST.	**07**
(b)	Write a short note on BIST timing, control, and design practices.	**07**

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